Claims

[c1] A semiconductor device structure, comprising:
at least first and second field effect transistors disposed on a substrate;
said first field effect transistor including a first spacer having a first width;
said second field effect transistor including a second spacer having a second width;
wherein said second spacer includes a first compressive stress material, and said structure further comprises a tensile stress material disposed on said at least first and second field effect transistors.

[c2] The structure as claimed in claim 1, wherein said first field effect transistor is an nFET and said second field effect transistor is a pFET.

[c3] The structure as claimed in claim 1, wherein said first width is less than said second width.

[c4] The structure as claimed in claim 1, wherein said structure is an inverter.

[c5] The structure as claimed in claim 1, wherein said structure includes a width transition region located approximately in a middle region between said transistors.

[c6] The structure as claimed in claim 1, wherein said first spacer includes an I-shaped part and said second spacer includes an L-shaped part.

[c7] The structure as claimed in claim 1, wherein said second spacer includes an L-shaped part and said first compressive stress material.

[c8] The structure as claimed in claim 1, wherein said first spacer includes said first compressive stress material.

[c9] The structure as claimed in claim 1, wherein said first width is a substantially uniform width in a range of about 10 nm to about 30 nm, and said second width has a maximum width in a range of about 50 nm to about 120 nm.

[c10] The structure as claimed in claim 1, wherein said first compressive stress material has a substantially uniform stress in a range of about -3E9 dynes/cm^2 to about -3E11 dynes/cm^2.

[c11] The structure claimed in claim 1, wherein said tensile stress material has a substantially uniform film thickness in a range of about 20 nm to about 100 nm and a substantially uniform stress in a range of approximately 4E9 dynes/cm^2 to approximately 4E11 dynes/cm^2.

[c12] The structure as claimed in claim 1, wherein said second spacer includes a second compressive stress material having a stress in a range of approximately -2E9 dynes/cm^2 to approximately 2E9 dynes/cm2.

[c13] The structure as claimed in claim 1, wherein said first compressive stress material is a dielectric.

[c14] The structure as claimed in claim 1, wherein said first compressive

stress material is silicon nitride.

[c15] The structure as claimed in claim 1, wherein said tensile stress material is SiN.

[c16] The structure as claimed in claim 1, wherein said first width is about 50 nm, and said second width has a maximum width of about 90 nm.

[c17] The structure as claimed in claim 1, wherein said tensile stress material is a layer having a substantially uniform thickness in a range of about 20 nm to about 100 nm.

[c18] A method for fabricating a semiconductor device structure, comprising:
providing a semiconductor substrate;
forming gate stacks on the substrate, extension spacers on the gate stacks, extension implants adjacent to the extension spacers, and an isolation region between at least two extension implants;
disposing a first compressive stress dielectric material onto the gate stacks, extension spacers, and extension implants;
disposing a second dielectric material with a low stress onto the first compressive stress dielectric material;
masking a first portion of the second dielectric material over one gate stack;
removing a second portion of the second dielectric material over another gate stack;
etching the first portion to form intermediate low stress spacers proximate to the one gate stack;
etching the first dielectric material to form narrow compressive spacers

proximate to the another gate stack and wide compressive spacers proximate to the one gate stack;
forming source and drain implants and silicides thereon;
disposing a tensile stress dielectric material over all the spacers.

[c19] The method as claimed in claim 18, wherein said step of disposing a first compressive stress dielectric material includes PECVD depositing silicon nitride.

[c20] The method as claimed in claim 18, wherein said step of disposing a tensile stress dielectric material includes CVD depositing a SiN layer.